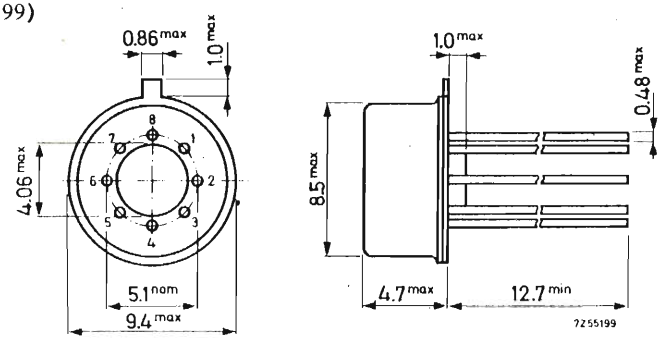
OPERATIONAL AMPLIFIER

The TAA241 is a silicon monolithic integrated d.c. amplifier in a TO-99 metal envelope for applications in the temperature range from 0 to 70 °C.

QUICK REFERENCE DATA				
Positive supply voltage	V_P		12	V
Negative supply voltage	$-V_N$		6	V
Characteristics at T_{amb} = 25 °C				
Voltage gain	G_v	typ.	3400	
Common mode rejection ratio	CMRR	typ.	92	dB
Input offset voltage drift	$\frac{\Delta V_{io}}{\Delta T}$	typ.	5	μV/°C
Differential input resistance	R_i	typ.	32	kΩ
Output resistance	R_o	typ.	200	Ω
Power dissipation	P_{tot}	typ.	90	mW

PACKAGE OUTLINE Dimensions in mm

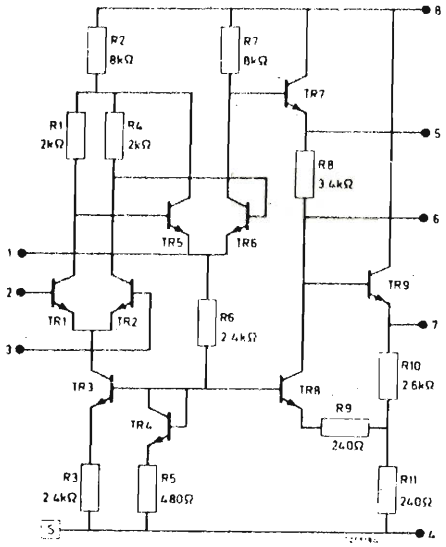
XA8 (TO-99)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages				
Total supply voltage	V_{8-4}	max.	21	V
Common mode voltage	V_i		−6 to +1.5	V
Differential mode voltage	V_{2-3}	max.	±5	V
Output current (peak value)	I_{OM}	max.	50	mA
Power dissipation up to T_{amb} = 70 °C	P_{tot}	max.	300	mW
Temperatures				
Operating ambient temperature	T_{amb}		0 to +70	°C
Storage temperature	T_{stg}		−65 to +150	°C

CIRCUIT DIAGRAM



1. Ground
2. Inverting input
3. Non-inverting input
4. Negative supply
5. Lead frequency compensation
6. Lag frequency compensation
7. Output
8. Positive supply

CHARACTERISTICS at $V_P = 12$ V; $-V_N = 6$ V; $T_{amb} = 25\ ^oC$

Voltage gain; $R_L \geq 100$ kΩ; $V_o = \pm 5$ V	G_v	2000 to 6000 typ.	3400	
Input offset voltage; $R_S \leq 2$ kΩ	V_{io}	typ. <	1.5 5	mV mV
Input bias current	I_i	typ. <	2.5 7.5	μA μA
Input offset current	I_{io}	typ. <	0.5 2	μA μA
Common mode rejection ratio at $f \leq 1$ kHz; $R_S \leq 2$ kΩ	CMRR	> typ.	70 92	dB dB
Input voltage range	V_i	−4 to +0.5		V
Supply current at $V_o = 0$	I_{tot}	typ. <	5 6.7	mA mA
Differential input resistance	R_i	> typ.	10 32	kΩ kΩ
Output resistance	R_o	typ. <	200 600	Ω Ω
Power dissipation at $V_o = 0$	P_{tot}	typ. <	90 120	mW mW

CHARACTERISTICS at $V_P = 12$ V; $-V_N = 6$ V; $T_{amb} = 0$ to $+70\ ^oC$ unless otherwise specified

Voltage gain; $R_L \geq 100$ kΩ; $V_o = \pm 5$ V	G_v	1500 to 7000		
Input offset voltage; $R_S \leq 2$ kΩ	V_{io}	<	6.5	mV
Average input offset voltage drift; $R_S = 50$ Ω	$\frac{\Delta V_{io}}{\Delta T}$	typ. <	5 20	μV/°C μV/°C
Input bias current at $T_{amb} = 0\ ^oC$	I_i	typ. <	4 12	μA μA
Input offset current	I_{io}	<	2.5	μA
Average input offset current drift at				
$T_{amb} = 0$ to $+25\ ^oC$	$\frac{\Delta I_{io}}{\Delta T}$	typ. <	6 20	nA/°C nA/°C
$T_{amb} = +25$ to $+70\ ^oC$	$\frac{\Delta I_{io}}{\Delta T}$	typ. <	4 10	nA/°C nA/°C
Common mode rejection ratio at $f \leq 1$ kHz; $R_S \leq 2$ kΩ	CMRR	> typ.	65 86	dB dB

CHARACTERISTICS (continued)

Supply voltage rejection ratio V_8 = +12 to +6 V; V_4 = −6 to −3 V; $R_S \leq 2$ kΩ	SVRR	typ. <	90 300	μV/V μV/V
Peak output voltage swing at $R_L \geq 100$ kΩ	V_{OM}	> typ.	±5 ±5.3	V V
$R_L \geq 10$ kΩ	V_{OM}	> typ.	±3.5 ±4	V V
Supply current at $V_o = 0$	Itot	typ. <	5 7	mA mA
Power dissipation at $V_o = 0$	P_{tot}	typ. <	90 125	mW mW