WIDEBAND DIFFERENTIAL LIMITING AMPLIFIER

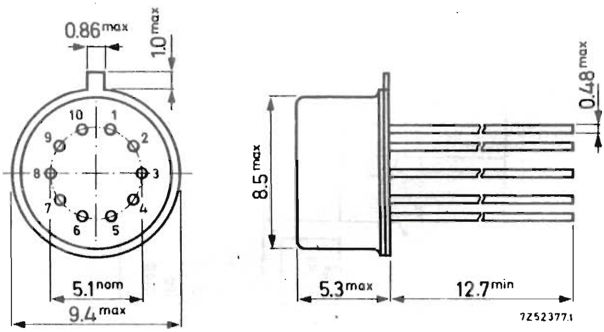
A monolithic integrated i.f. amplifier for f.m. signals. Differential amplification with current-driven long-tailed pairs gives high a.m. rejection, making the amplifier usable in conjunction with very simple f.m. detectors. The TAA350 can be driven either symmetrically or asymmetrically.

QUICK REFERENCE DATA

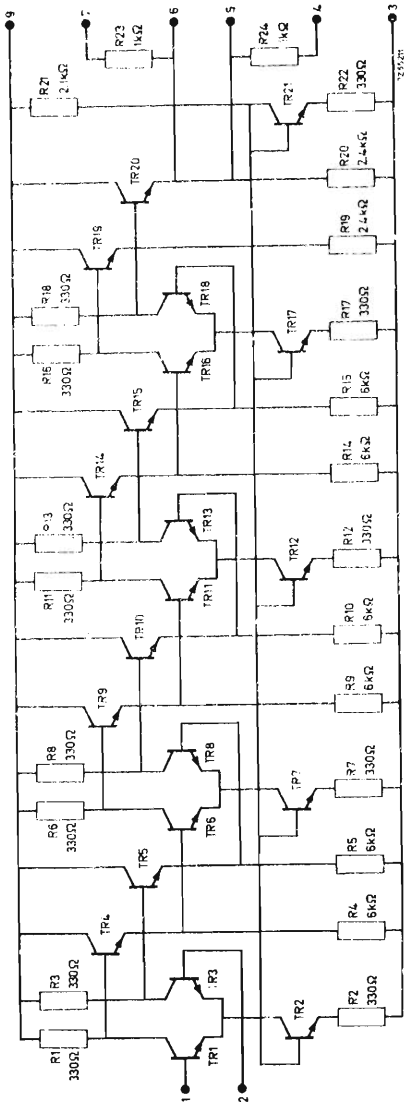
Supply voltage		6	V
Frequency		5.5	MHz
Total current	typ.	20	mA
Power gain	typ.	80	dB
Input limiting voltage	typ.	100	μV
Frequency response (−3 dB)	typ.	12	MHz
Output impedance	typ.	75	Ω

PACKAGE OUTLINE Dimensions in mm

XA10 (TO-74; reduced height)



CIRCUIT DIAGRAM



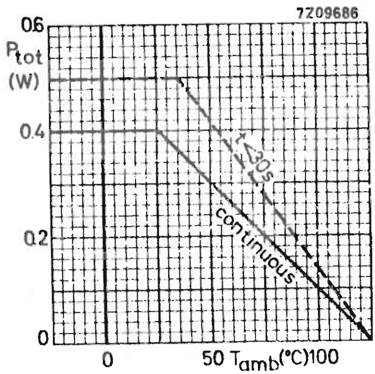
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Pin No.1 voltage at $V_{2-3} = V_{1-3}$; $V_{1-3} \leq V_{9-3}$	V_{1-3}	0 to +10	V
Pin No.2 voltage at $V_{1-3} = V_{2-3}$; $V_{2-3} \leq V_{9-3}$	V_{2-3}	0 to +10	V
Pin No.4 voltage (do not apply an external voltage source)	V_{4-3}	0 to +10	V
Pin No.5 voltage at $\|I_5\| < 20$ mA; $V_{5-3} \leq V_{9-3}$	V_{5-3}	0 to +10	V
Pin No.6 voltage at $\|I_6\| < 20$ mA; $V_{6-3} \leq V_{9-3}$	V_{6-3}	0 to +10	V
Pin No.7 voltage (do not apply an external voltage source)	V_{7-3}	0 to +10	V
Pin No.9 voltage with lower d.c. potential at all other terminals	V_{9-3}	0 to +10	V

Do not connect pins 8 and 10.
The maximum signal voltage between pins 1 and 2 is 6 V.

Total power dissipation



Temperatures

Storage temperature	T_{stg}	−25 to +125	°C
Operating ambient temperature	T_{amb}	−25 to +125	°C

CHARACTERISTICS T_{amb} = 25 °C unless otherwise specified

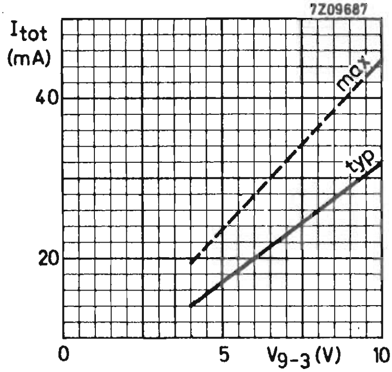
Because the TAA350 has a low ohmic output impedance and it mostly is driven by a bandpass or parallel tuned filter, four-pole hybrid k parameters have been introduced.

The four-pole equations are:

$$I_i = k_i V_i + k_r I_o$$

$$V_o = k_f V_i + k_o I_o$$

Total current (d.c.) [1]



k parameters (see pages 6 to 9)

f = 5.5 MHz; V_{9-3} = 6 V

Input conductance (input pin 2)	g_i	typ.	400	$\mu\Omega^{-1}$
Input susceptance (input pin 2)	b_i	typ.	550	$\mu\Omega^{-1}$
Reverse current transfer ratio (output pin 6, input pin 2) [2]	$\lvert k_r \rvert$	typ.	-90	dB
Small signal voltage gain (input pin 2, output pin 6)	$\lvert k_f \rvert$	typ.	67	dB
Real part of output impedance (output pin 6)	$Re(k_o)$	typ.	75	Ω
Imaginary part of output impedance (output pin 6)	$Im(k_o)$	typ.	20	Ω

f = 10.7 MHz; V_{9-3} = 6 V

Reverse current transfer ratio (output pin 6, input 2) [2]	$\lvert k_r \rvert$	typ.	-80	dB
Small signal voltage gain (input pin 2, output pin 6)	$\lvert k_f \rvert$	typ.	65	dB

Input limiting voltage (see pp 5 and 8) [3]

f = 5.5 MHz; V_{9-3} = 6 V	$V_{i\,lim}$	typ.	100	μV

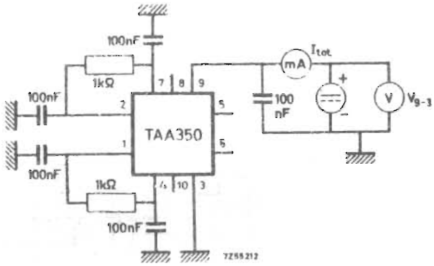
[1]) The power dissipation is obtained from $V_{9-3} \times I_{tot}$.

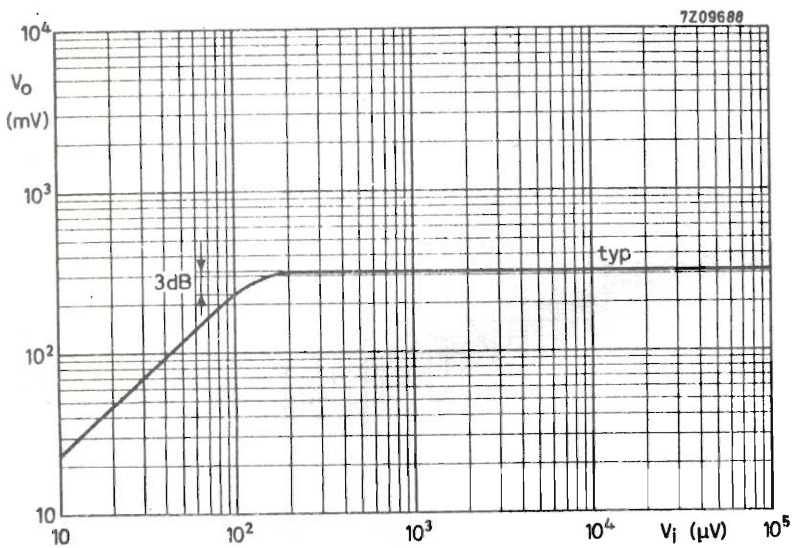
[2]) The output is considered open for $R_L \geq 10$ kΩ and $C_L \leq 10$ pF.

[3]) $V_{i\,lim}$ is defined as the input signal voltage which decreases the output voltage 3 dB of its max. level (see also page 5).

CHARACTERISTICS (continued)

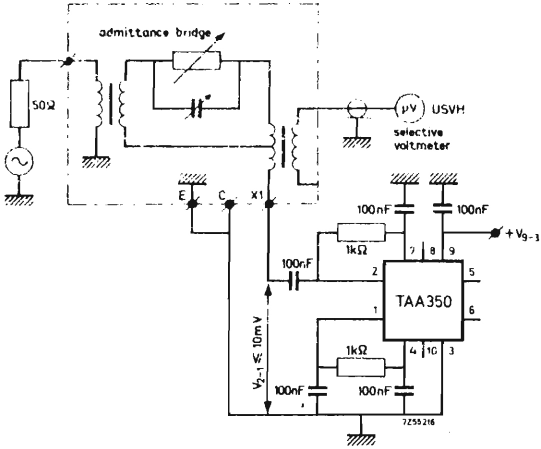
Test circuit for measuring $I_{tot} = f(V_{9-3})$

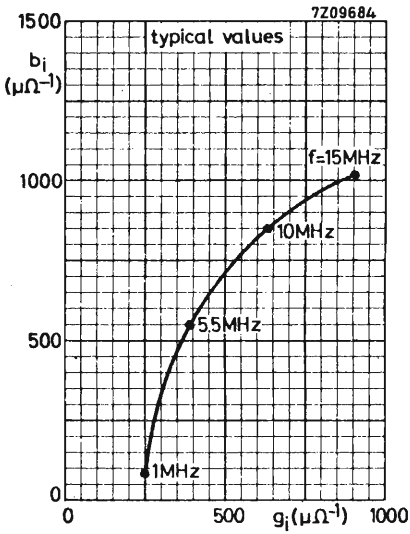




CHARACTERISTICS (continued)

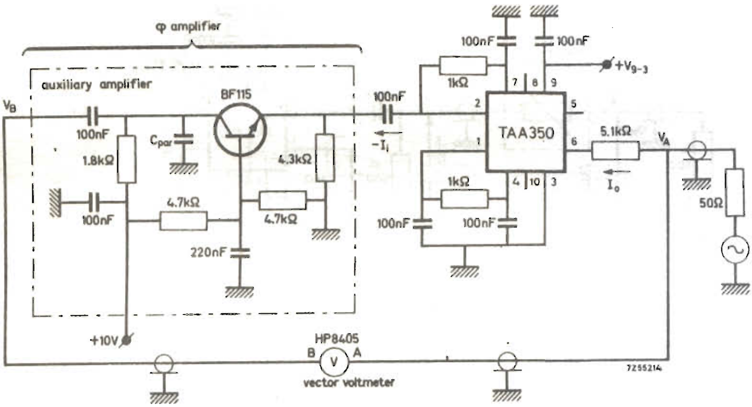
Test circuit for measuring the input characteristic

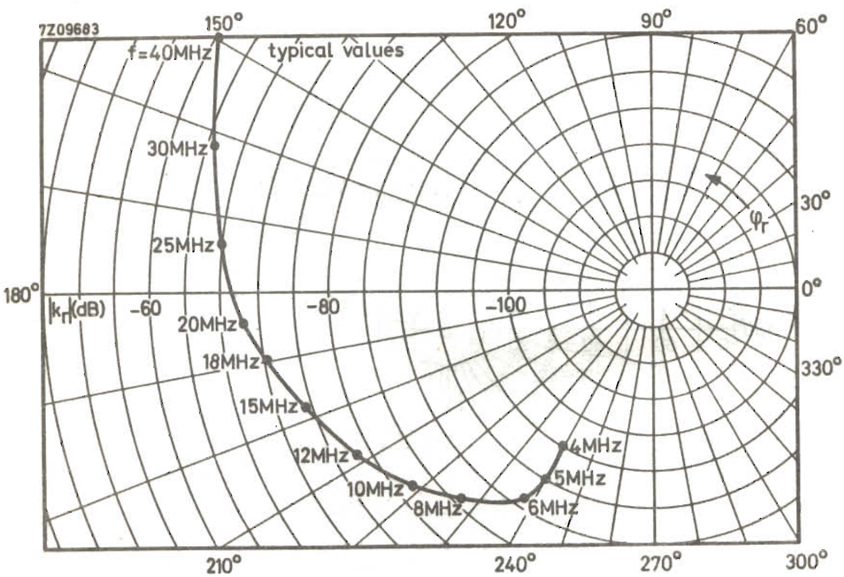




CHARACTERISTICS (continued)

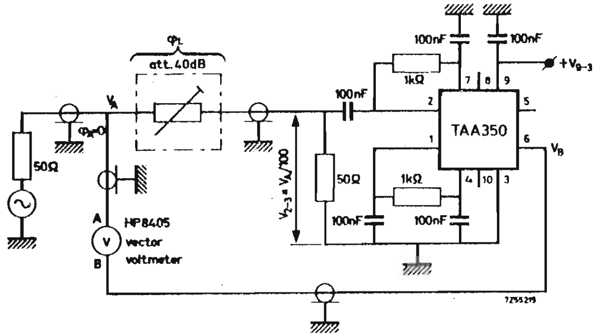
Test circuit for measuring the reverse current transfer ratio





CHARACTERISTICS (continued)

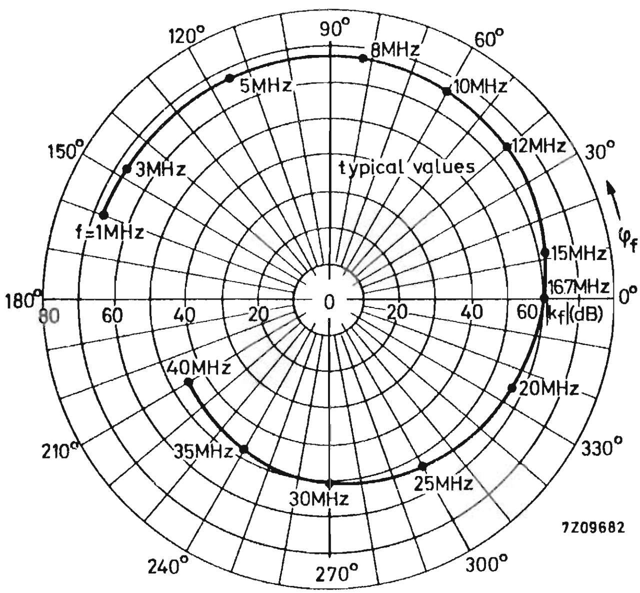
Test circuit for measuring the small signal voltage gain and the input limiting voltage



$$\overline{k_f} = (20 \log \frac{V_B}{V_A} + 40\ dB) . e^{j(\varphi_B - \varphi_1)}$$

$V_{i\ lim} = V_{Bmax} - 3\ dB$

To obtain V_{Bmax}: V_A is increased until V_B is constant



CHARACTERISTICS (continued)

Test circuit for measuring the output characteristic