SGS **TDA2002**

LINEAR INTEGRATED CIRCUIT

8W CAR RADIO AUDIO AMPLIFIER

The TDA 2002 is a class B audio power amplifier in Pentawatt® package designed for driving low impedance loads (down to 1.6Ω). The device provides a high output current capability (up to 3.5A), very low harmonic and cross-over distortion. In addition, the device offers the following features:

- very low number of external components
- assembly ease, due to Pentawatt® power package with no electrical insulation requirement
- space and cost saving
- high reliability
- flexibility in use
- complete safety during operation due to protection against:
  a) short circuit; b) thermal over range; c) fortuitous open ground; d) polarity inversion (V_s max= 12V); e) load dump voltage surge.

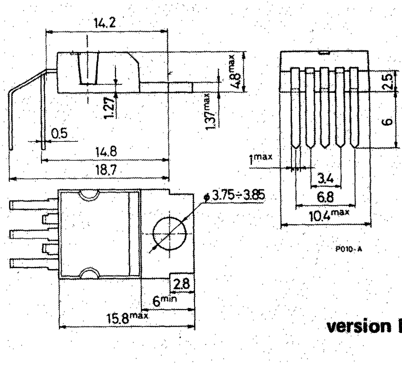
ABSOLUTE MAXIMUM RATINGS

V_s	Peak supply voltage (50 ms)	40	V
V_s	DC supply voltage	28	V
V_s	Operating supply voltage	18	V
I_o	Output peak current (repetitive)	3.5	A
I_o	Output peak current (non repetitive)	4.5	A
P_{tot}	Power dissipation at T_{case}= 90°C	15	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

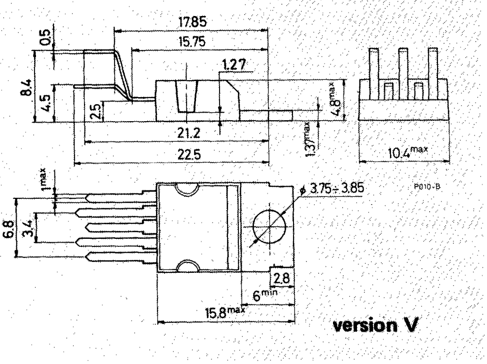
ORDERING NUMBERS: TDA 2002 H
TDA 2002 V

MECHANICAL DATA

Dimensions in mm

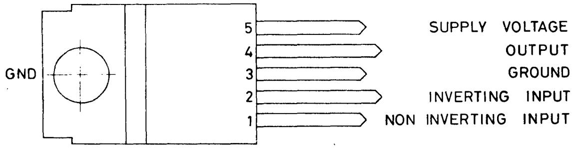


version H



version V

CONNECTION DIAGRAM
(top view)



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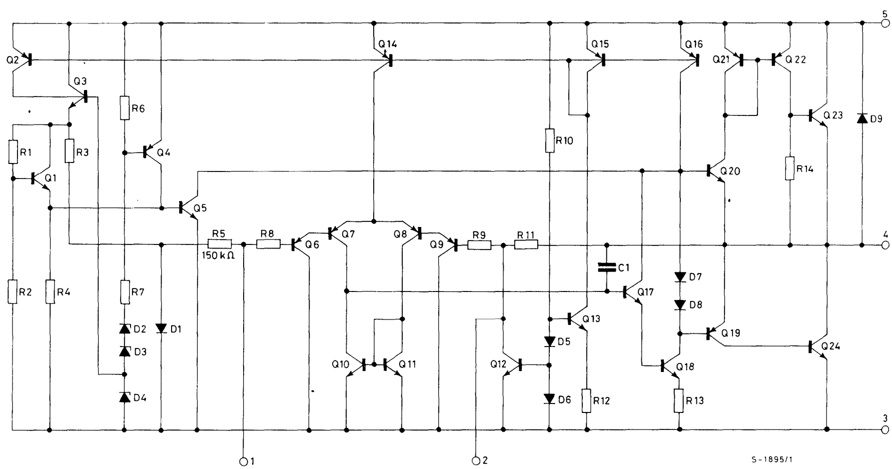
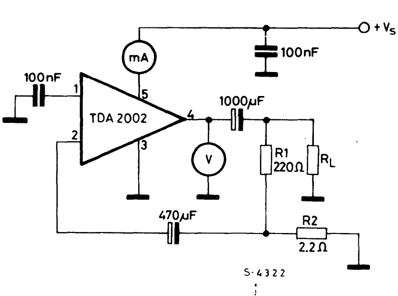
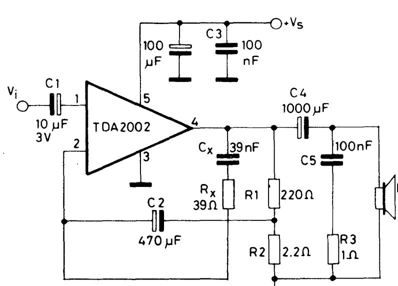
SCHEMATIC DIAGRAM



DC TEST CIRCUIT



AC TEST CIRCUIT



$R_x = 20 \cdot R2$; $C_x = \frac{1}{2\pi B R1}$

S-4323

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 14.4V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS (Refer to DC test circuit)							
V_s	Supply voltage			8		18	V
V_o	Quiescent output voltage (pin 4)			6.4	7.2	8	V
I_d	Quiescent drain current (pin 5)				45	80	mA
AC CHARACTERISTICS (Refer to AC test circuit, G_v = 40 dB)							
P_o	Output power	d = 10%	f = 1 kHz				
			R_L = 4Ω	4.8	5.2		W
			R_L = 2Ω	7	8		W
		V_s = 16V	R_L = 4Ω		6.5		W
			R_L = 2Ω		10		W
$V_{i\,(rms)}$	Input saturation voltage			600			mV
V_i	Input sensitivity		f = 1 kHz				
		P_o = 0.5W	R_L = 4Ω		15		mV
		P_o = 0.5W	R_L = 2Ω		11		mV
		P_o = 5.2W	R_L = 4Ω		55		mV
		P_o = 8W	R_L = 2Ω		50		mV
B	Frequency response (-3 dB)	R_L = 4Ω	P_o = 1W	40 to 15 000			Hz
d	Distortion		f = 1 kHz				
		P_o = 0.05 to 3.5W	R_L = 4Ω		0.2		%
		P_o = 0.05 to 5W	R_L = 2Ω		0.2		%
R_i	Input resistance (pin 1)	f = 1 kHz		70	150		kΩ
G_v	Voltage gain (open loop)	R_L = 4Ω	f = 1 kHz		80		dB
G_v	Voltage gain (closed loop)	R_L = 4Ω	f = 1 kHz	39.5	40	40.5	dB
e_N	Input noise voltage (*)				4		μV
i_N	Input noise current (*)				60		pA
η	Efficiency		f = 1 kHz				
		P_o = 5.2W	R_L = 4Ω		68		%
		P_o = 8W	R_L = 2Ω		58		%
SVR	Supply voltage rejection	R_L = 4Ω R_g = 10 kΩ f_{ripple} = 100 Hz		30	35		dB

(*) Filter with noise bandwidth: 22 Hz to 22 KHz.

Fig. 1 - Quiescent output voltage vs. supply voltage

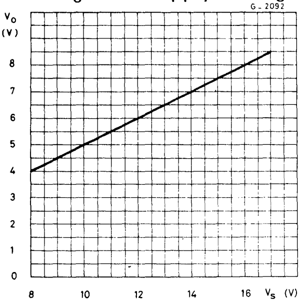


Fig. 2 - Quiescent drain current vs. supply voltage

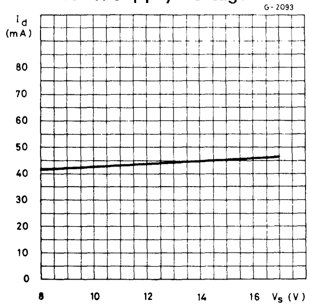


Fig. 3 - Output power vs. supply voltage

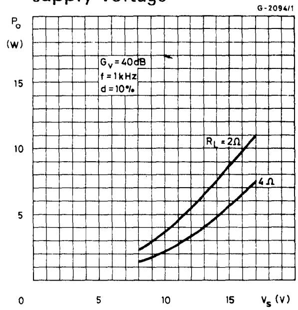


Fig. 4 - Output power vs. load resistance R_L

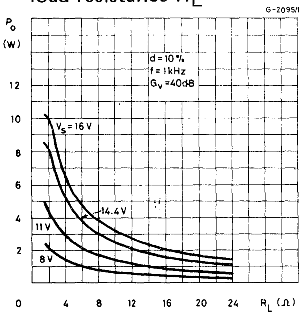


Fig. 5 - Input voltage vs. voltage gain (R_L = 4Ω)

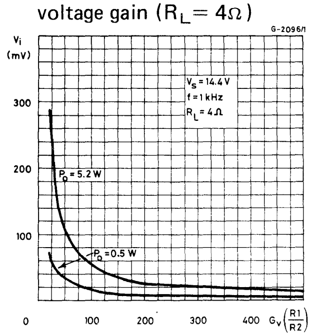


Fig. 6 - Input voltage vs. voltage gain (R_L = 2Ω)

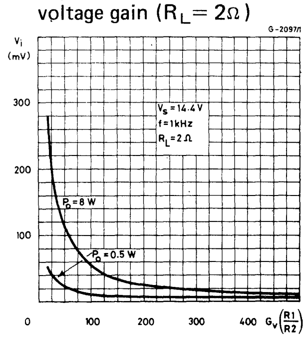


Fig. 7 - Distortion vs. output power

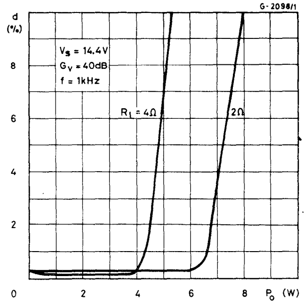


Fig. 8 - Distortion vs. frequency

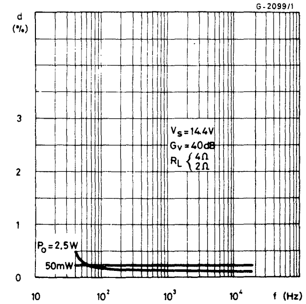


Fig. 9 - Supply voltage rejection vs. voltage gain

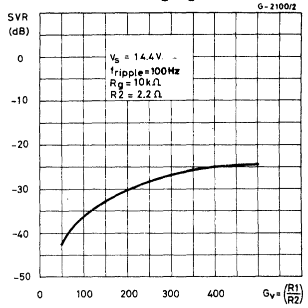


Fig. 10 - Supply voltage rejection vs. frequency

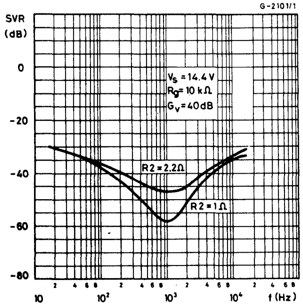


Fig. 11 - Power dissipation and efficiency vs. output power ($R_L = 4\Omega$)

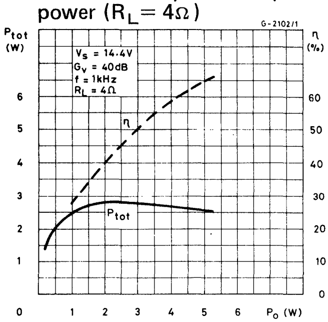


Fig. 12 - Power dissipation and efficiency vs. output power ($R_L = 2\Omega$)

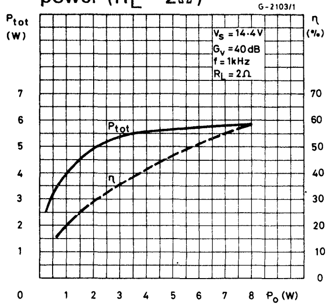


Fig. 13 - Maximum power dissipation vs. supply voltage (sine wave operation)

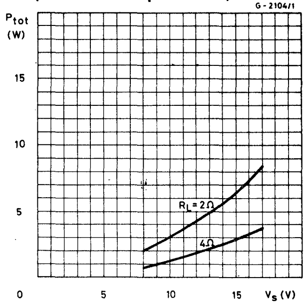


Fig. 14 - Maximim allowable power dissipation vs. ambient temperature

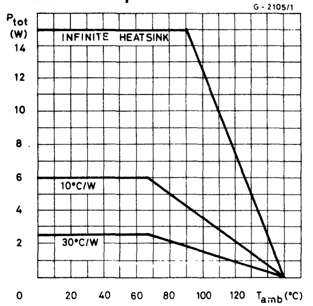
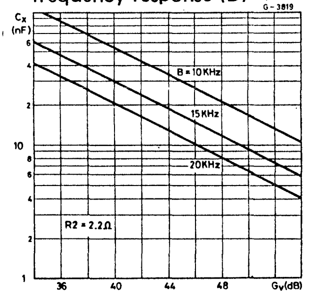
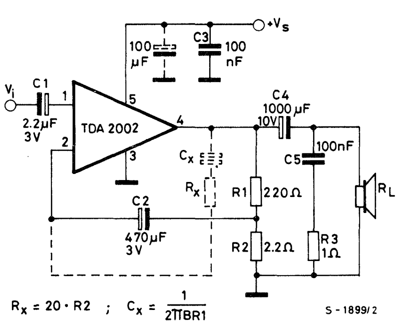


Fig. 15 - Values of capacitor (C_X) for different values of frequency response (B)



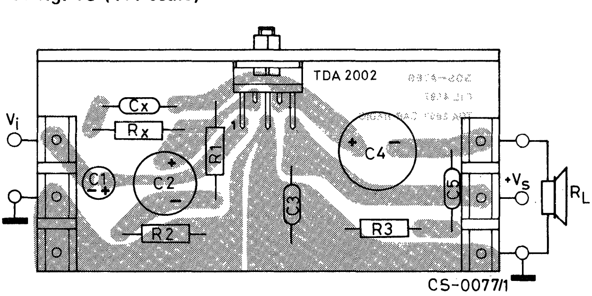
APPLICATION INFORMATION

Fig. 16 - Application circuit



$R_x = 20 \cdot R2$; $C_x = \frac{1}{2\pi B R1}$

Fig. 17 - P.C. board and component layout for the circuit of fig. 16 (1:1 scale)



LOAD DUMP VOLTAGE SURGE PROTECTION

The TDA 2002 has a circuit which enables it to withstand a voltage pulse train, on pin 5, of the type shown in fig. 18. If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 5, in order to assure that the pulses at pin 5 will be held within the limits shown in fig.18.

A suggested LC network is shown in fig. 19. With this network, a train of pulses with amplitude up to 120V and width of 2 ms can be applied at point A. This type of protection is ON when the supply voltage (pulsed or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 18

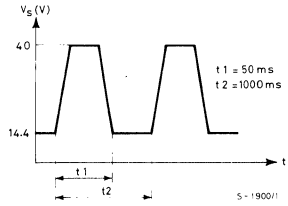
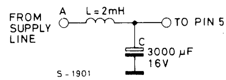


Fig. 19



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood
2) the heat-sink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced (figs. 20 and 21)

Fig. 20 - Output power and drain current vs. case temperature ($R_L = 4\Omega$)

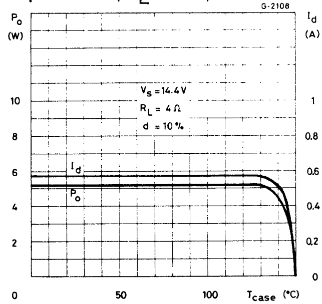
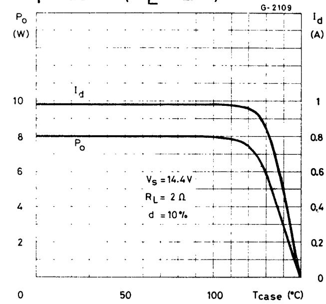


Fig. 21 - Output power and drain current vs. case temperature ($R_L = 2\Omega$)



PRACTICAL CONSIDERATIONS

Printed circuit board

The layout shown in fig. 17 is recommended. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground of the output through which a rather high current flows.

Assembly suggestion

No electrical insulation is needed between the package and the heat-sink. Pin length should be as short as possible. The soldering temperature must not exceed 260°C for 12 seconds.

Application suggestions

The recommended component values are those shown in the application circuits of fig. 16. Different values can be used. The following table is intended to aid the car-radio designer.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
C1	2.2 μF	Input DC decoupling		Noise at switch-on, switch-off
C2	470 μF	Ripple rejection		Degradation of SVR
C3	0.1 μF	Supply bypassing		Danger of oscillation
C4	1000 μF	Output coupling to load		Higher low frequency cutoff
C5	0.1 μF	Frequency stability		Danger of oscillation at high frequencies with inductive loads
C_X	$\cong \frac{1}{2 \pi B R1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
R1	$(G_V-1) \cdot R2$	Setting of gain		Increase of drain current
R2	2.2 Ω	Setting of gain and SVR	Degradation of SVR	
R3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_X	$\cong$ 20 R2	Upper frequency cutoff	Poor high frequency attenuation	Danger of oscillation